- each of said processors has a processor identification register which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register.

3. (Amended)A computer system as claimed in Claim 2, wherein said reset state is a state asserted in said computer system following boot or re-boot.

6. (Amended)A computer system as claimed Claim 1, wherein said common predefined data value is an all zeros value.

7. (Amended)A computer system as claimed in Claim 1, wherein each of said processors further includes

- a read only register having stored therein said processor identification data.

8. (Amended)A computer system as claimed in Claim 7, wherein said processor identification data stored in said read only register is loaded, upon initialisation into said processor identification register.

9. (Amended)A computer system as claimed in Claim 1, wherein said common predefined value is a processor identification of one of the processors of said computer system, said processor identification of each of said processors being matched.

10. (Amended)A processor for use in a processing set forming part of a fault tolerant computer system that includes a plurality of processing sets, said processor comprising

- an interface for communication with an I/O bus, and
- a processor identification register which is read/writeable and has stored in said register data representative of a processor identification, wherein said processor is responsive to a masking condition, to write a common predefined data value

received via said I/O bus into said processor identification register, wherein said predefined data value is common to said processing sets and is operable to mask said processor identification.

11. (Amended)A processor as claimed in Claim 10, comprising

- a read only register having stored therein said processor identification data, wherein said processor identification data stored in said read only register is loadable, upon initialisation into said processor identification register.

12. (Amended)A method of operating a fault tolerant computer system comprising a plurality of processing sets, each of which processing sets is connected to a bridge, each of said processing sets having at least one processor, said method comprising the steps of;

a) detecting a predetermined condition representative of a state in which said processor identification is present in a processor identification register of said processor; and

b) loading a common predefined data value into said processor identification register of each of said processors, which predefined data value [has an effect of masking] is common to said processing sets and is operable to mask said processor identification.

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15. (Amended)A method of operating a fault tolerant computer system as claimed in Claim 12, comprising

detecting an error condition of at least one of said plurality of processing sets, and

if said error condition is detected performing the step of loading said common predefined data value in said processor identification register of said at least one processor of the processing set which has said detected error.

16. (Amended)A method of operating a fault tolerant computer system comprising a plurality of processing sets, each having at least one processor, and a bridge coupled to each of said processing sets and operable to monitor a step locked operation of said processing sets, said method comprising the steps of